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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,246	03/09/2004	Salman Akram	MIO 0069 VA/40509.245	2136

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EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,246	AKRAM ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1,3-7,9-15 and 17-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,8 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/17/05,11/15/04*. 7/16/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS cont. 6/10/04*.

DETAILED ACTION

This office action is in response to the election filed April 22, 2005.

Election/Restrictions

Applicant's election of invention I, and Species I drawn to claims 2, 8 and 16 in the reply filed on April 22, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 2, 8, 16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,507,107 in view of with Distefano (U.S. 6,075,289) and Suzuki et al (US 5,532,910).

'107 claims:

(cl. 2, 8) a first semiconductor die having a first active surface, said first active surface including at least one conductive bond pad; a second semiconductor die (40) defining a second active surface, said second active surface including at least one conductive bond pad; an intermediate substrate comprising a network of conductive contacts formed thereon, said substrate positioned between said first and second die, such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second active surface, said intermediate substrate includes a passage and one of the first and second die active surface aligned with the passage, a printed circuit board positioned such that a first surface of the board faces the intermediate substrate; a plurality of topographic contacts extending from said intermediate substrate to said first surface of said board (CLM 1 of '107);

(cont. cl. 8) wherein said first die is electrically connected to the intermediate substrate by a topographic contact extending form said first active surface to said intermediate with said second die secured to the second surface of the intermediate substrate, such that the conductive pads of the second die is aligned with the passage and said second die is electrically connected to the intermediate substrate by at least one conductive line extending form the bond pad of the second die through said passage and to contact first surface of the intermediate substrate (CLM 6-9 of '107);

(cl. 16) assembly is in a computer system comprising a programmable controller, memory unit wherein the unit comprises a printed circuit board (CLM 2 of '107).

'107 does not claim specifically that its intermediate substrate is a single layer, a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate, or at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die , said second semiconductor die, or a topographic contact.

Distefano (Fig.2) discloses a single layer intermediate substrate (48) and cap including a heat sink coupled to at least one die major surface (i.e. horizontal surface) with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate.

It would have been obvious to one of ordinary skill in the art to form the intermediate substrate of '107 as a single layer in order to provide a substrate as required by '107and further to incorporate a cap including a heat sink to package of '107 in order to provide thermally enhanced packages as taught by Distefano (Title).

Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die Suzuki (Col. 1, Lines 48).

It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including '107 in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

With respect to the placement of the capacitor, such that a thickness dimension of said decoupling capacitor accommodated in a space defined by a thickness dimension of one of said first semiconductor[1], it would have been obvious, since the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results. *See e.g. In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

[1] Capacitors are known to be placed in various parts of a package as illustrated in Watanabe et al. (U.S. 2002/0074669) and Kweon et al. (U.S. 5,656,856).

Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination with Distefano (U.S. 6,075,289) and Suzuki et al (US 5,532,910).

Lo (Fig. 1) discloses:

(cl. 2, 8) a first [*alternate second* for cl. 8] semiconductor die (26) having a first active surface (i.e. top portion), said first active surface including at least one conductive bond pad (32); a second [*alternate first* for cl. 8] semiconductor die (40) defining a second active surface (i.e. bottom surface), said second active surface including at least one conductive bond pad (40a); a single intermediate substrate (12) comprising a network of conductive contacts (18) formed thereon, said substrate positioned between said first and second die, such that a first surface [*alternate second* for cl. 8] of said intermediate substrate (bottom) faces said first active surface and such that a second [*alternate first* for cl. 8] surface (top portion) of said intermediate substrate faces said second active surface (bottom portion), said intermediate substrate includes a passage (defined by item 24) and one of the first and second die active surface aligned with the passage (i.e. die, 26), a printed circuit board (100) positioned such that a first surface (i.e. top portion) of the board faces the intermediate substrate; a plurality of topographic contacts (48) extending from said intermediate substrate to said first surface of said board;

(cont. cl. 8) wherein said first die is electrically connected to the intermediate substrate by a topographic contact (52) extending form said first active surface to said intermediate with said second die secured (34) to the second surface of the intermediate substrate, such that the conductive pads (32) of the second die is aligned

with the passage and said second die is electrically connected to the intermediate substrate by at least one conductive line (38) extending form the bond pad of the second die through said passage and to contact first surface of the intermediate substrate.

Lo does not discloses a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate, or at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die , said second semiconductor die, or a topographic contact.

Distefano (Fig. 2) discloses a cap including a heat sink coupled to at least one die major surface (i.e. horizontal surface) with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate.

It would have been obvious to one of ordinary skill in the art to incorporate a cap including a heat sink to package of Lo in order to provide thermally enhanced packages as taught by Distefano (Title).

Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die Suzuki (Col. 1, Lines 48).

It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including Lo in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

With respect to the placement of the capacitor, such that a thickness dimension of said decoupling capacitor accommodated in a space defined by a thickness dimension of one of said first semiconductor[1], it would have been obvious, since the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results. *See e.g. In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098), Distefano (U.S. 6,075,289) and Suzuki et al (US 5,532,910) as applied to claim 2 and further in combination with Corisis et al. (U.S. 2002/0135066).

Neither Lo, Distefano nor Suzuki appears to show its board is resident in a computer system, comprising a programmable controller, memory unit including board.

Corisis (Fig. 12) utilizes a board in resident in a computer system ("electronic system"; Par. 0024), comprising a programmable controller (132), memory unit including board (138).

It would have been obvious to one of ordinary skill in the art to incorporate the board of the prior art in a computer system comprising a programmable controller, memory unit including board in order to form an electronic system as taught by Corisis (Par. 0024).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art disclose in: Phelps Jr. et al. (U.S. 4,878,108), Ohki (U.S. 6,143,590), Lin et al. (U.S. 6,849,942) and Desai et al. (U.S. 6,166,434) the use of a cap including a heat sink engaging a mounting zone.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
July 5, 2005

CARL WHITEHEAD, JR.
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